AMULET3i

An Asynchronous

System-on-Chip

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AMULET3i

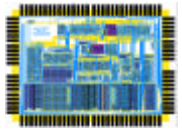
- What is it?
  - Asynchronous ARM
  - Asynchronous memory
  - Asynchronous bus
  - ...
- Why do it?
  - Low power
  - Low EMI
  - Improved security (?)

Motivation for asynchronous design

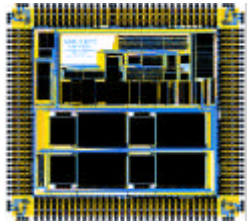
- low power
  - clocks cause unnecessary activity
- electromagnetic compatibility (EMC)
  - clocks cause coherent, periodic activity
- modularity
  - ‘object-oriented’ hardware
- performance
  - ‘typical’ rather than ‘worst-case’

The AMULET microprocessors

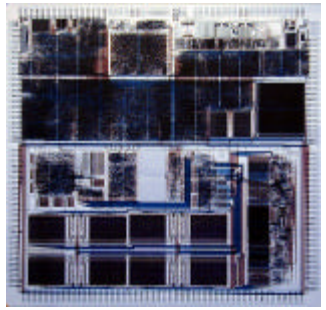
- AMULET1 (1994)
  - demonstrated feasibility



- AMULET2e (1996)
  - Demonstrated merits

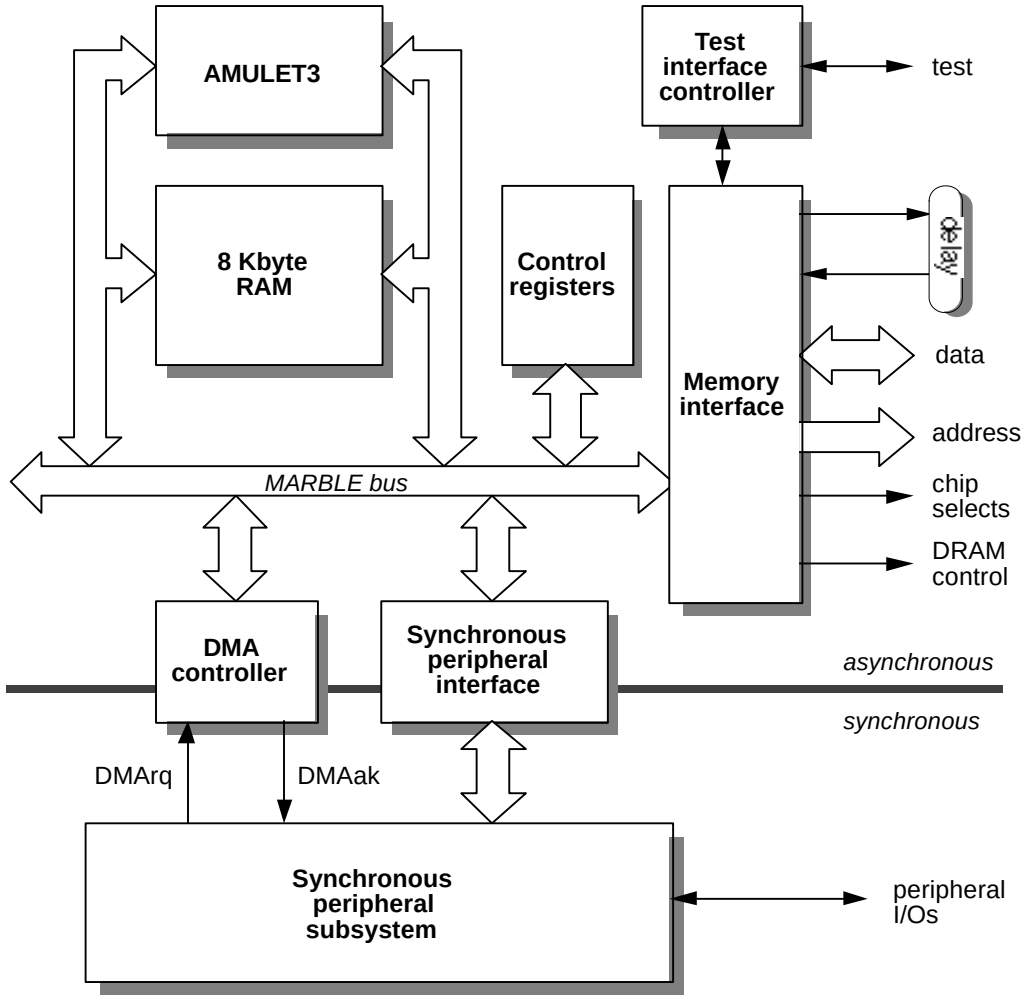


- AMULET3 (2000)
  - demonstrates commercial viability of asyncronous SoC design

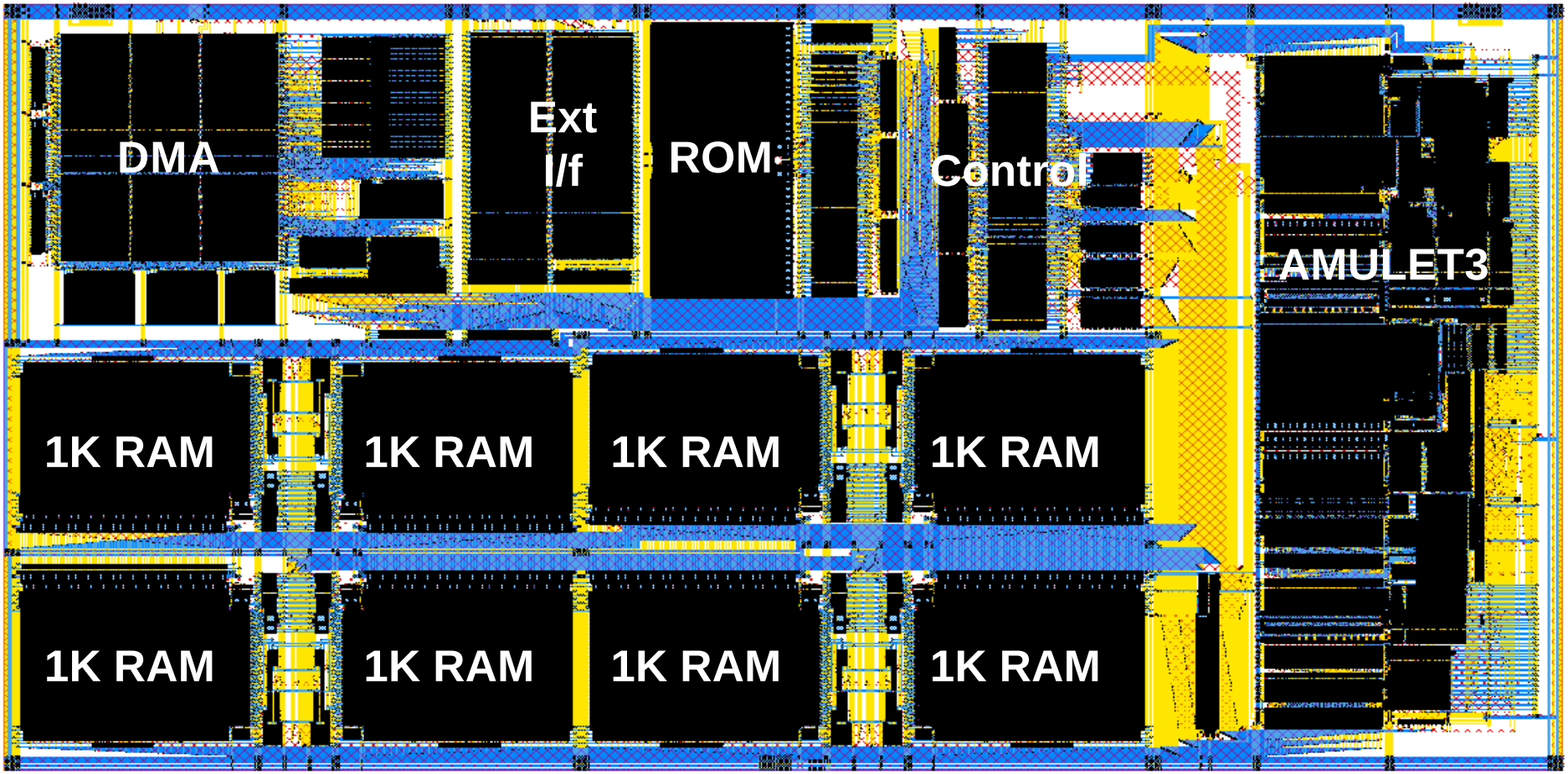


AMULET3i asynchronous 'island'

- AMULET3 microprocessor
- 8 Kbytes RAM
- 16 Kbytes ROM
- DMA controller
- Memory interface
- MARBLE -
  - Asynchronous bus
- Synchronous bridge
- Test interface



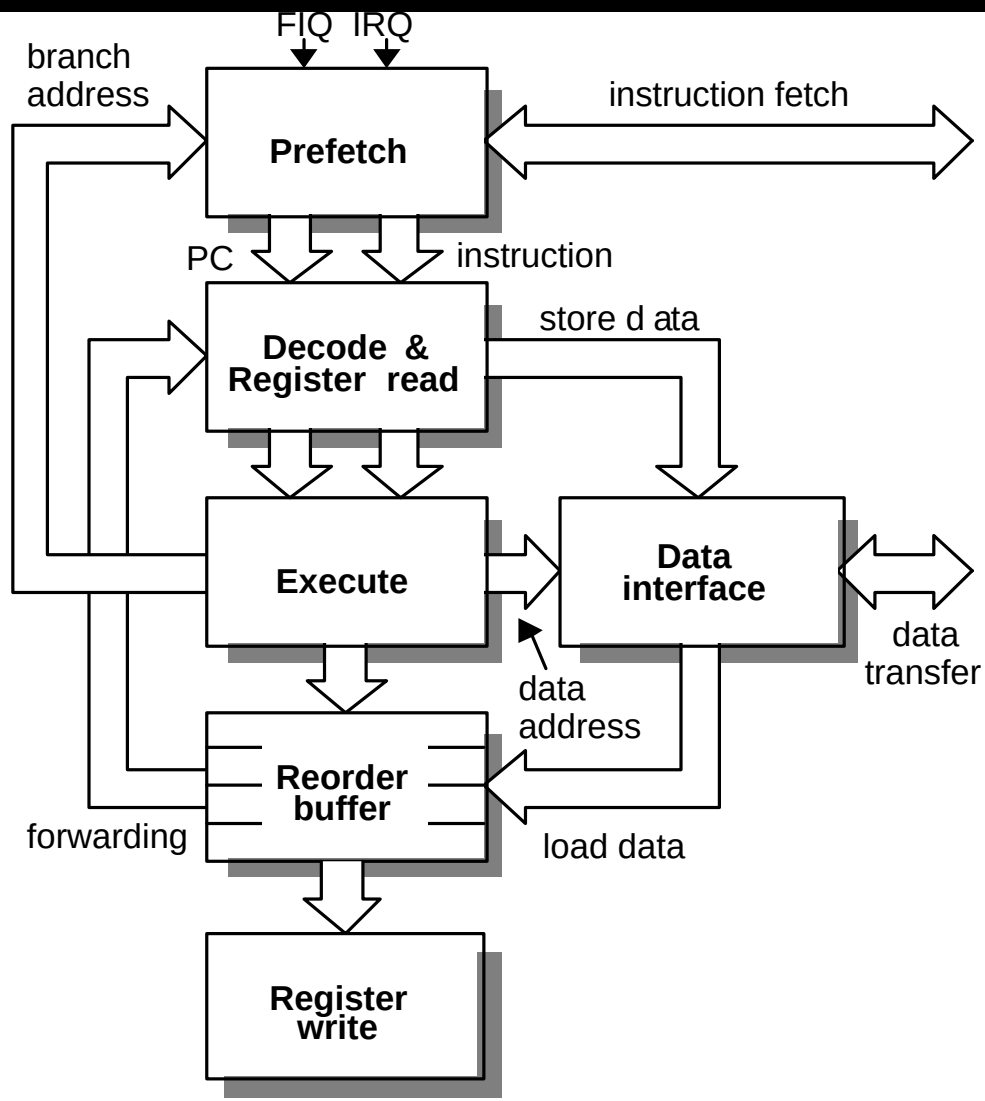
AMULET3i


DMA
Ext
I/f
ROM
Control
AMULET3
1K RAM
1K RAM
1K RAM
1K RAM
1K RAM
1K RAM
1K RAM
1K RAM

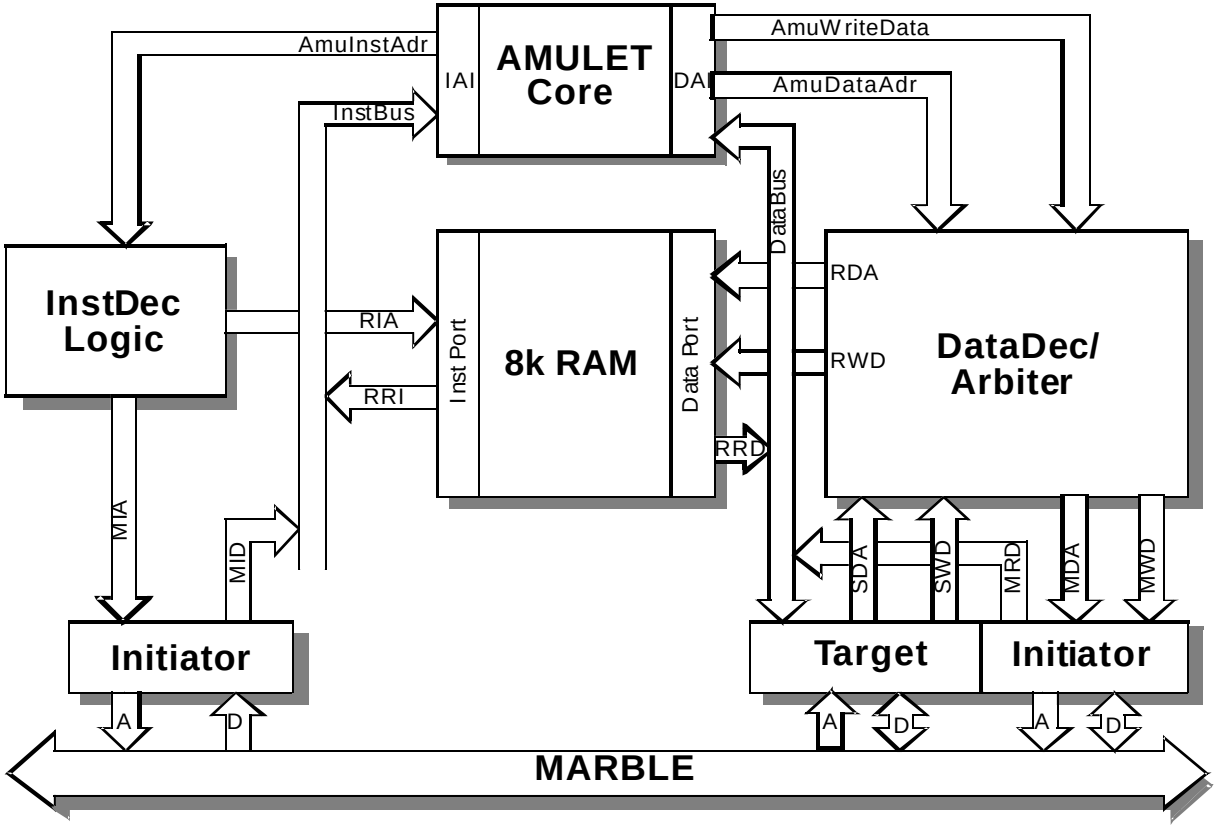
AMULET3 microprocessor

Features:

- Harvard bus interface
- Branch prediction
  - fetch suppression
- Both ARM & Thumb
- Register forwarding
- Out-of-order completion

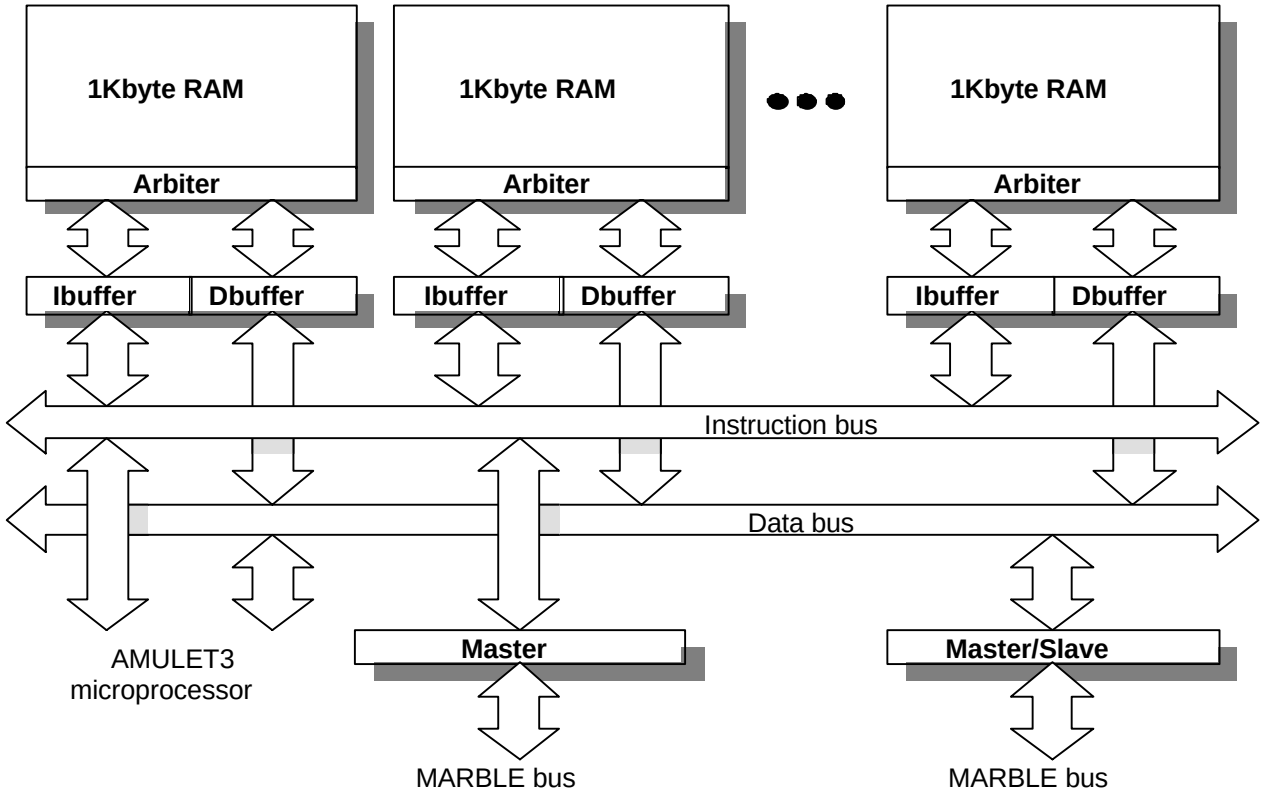


Memory system



- RAM *appears* to be dual-ported
- Instruction bus is simpler ⇒ faster

Memory structure



- Unified RAM model
  - arbitration within blocks
- Dual-port efficiency (nearly)
  - extra ‘block buffer’ help

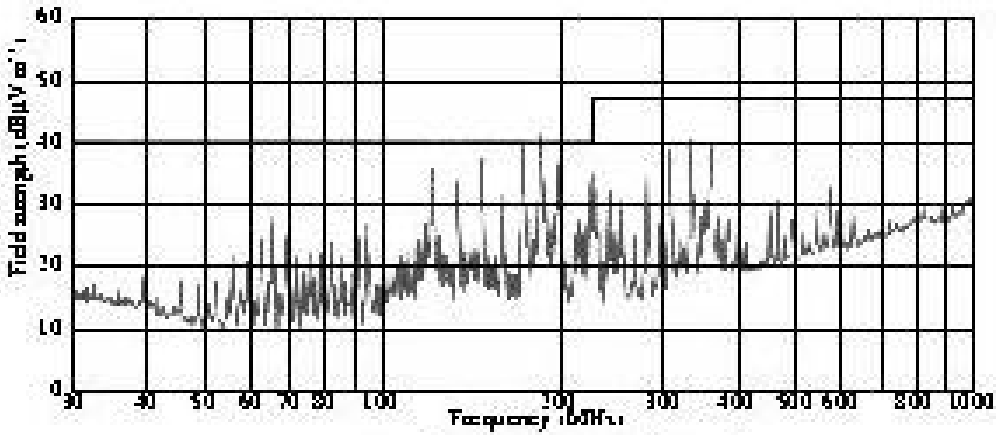
DMA controller/Balsa

- Fairly standard peripheral
  - High performance *not* required
- First application of Balsa
  - asynchronous synthesis language
- About 70 000 transistors
  - Registers hand laid-out
  - Control synthesized
- Usual synthesis benefits ...

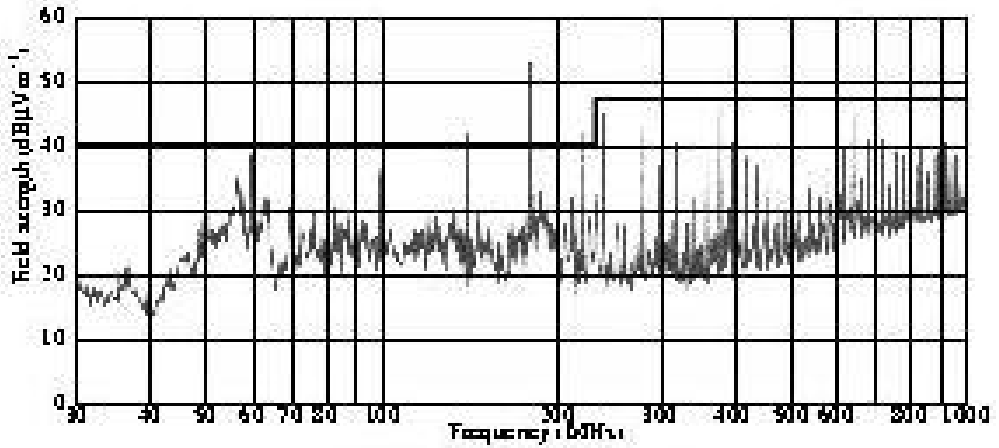
AMULET2e EMC tests

Previous results ...

- test card meets EN 55022 without special measures
- clocked card exceeds limit at several frequencies



AMULET2e evaluation board



ARM60 "PIE" board

Chip statistics

Transistor count

- AMULET3 113 000
- RAM 504 000
- DMA controller 70 000
- Memory Interface 26 000
- Total 800 000

Geometry

- 0.35 um, 3-layer metal (Generic ASIC rules)

Area

- AMULET3i ~25mm^2
- AMULET3 ~3mm^2

Performance

- Simulations at 3.3V, 25°C
- 105 native MIPS (peak)
- 102 MIPS Dhrystone 2.1
- 215mW average power
- Processor core 130mW

Performance

- Processor alone
  - AMULET3 110-140MIPS 780 MIPS/W 3mm^2
  - ARM9 120 MHz 800 MIPS/W 3mm^2
- Bus bandwidth
  - Instruction bus 105/83 Mwords/s (‘hit’/‘miss’)
  - Data bus 77/63 Mwords/s (‘hit’/‘miss’)
  - MARBLE 55/85 Mwords/s (one/all masters)

Comments

- AMULET3i is about 2.5x faster than AMULET2e
  - 1.7x when normalized for process
- The performance is limited by memory bandwidth
- The processor is within a few % of a comtemporary, synchronous ARM in performance, power and silicon area

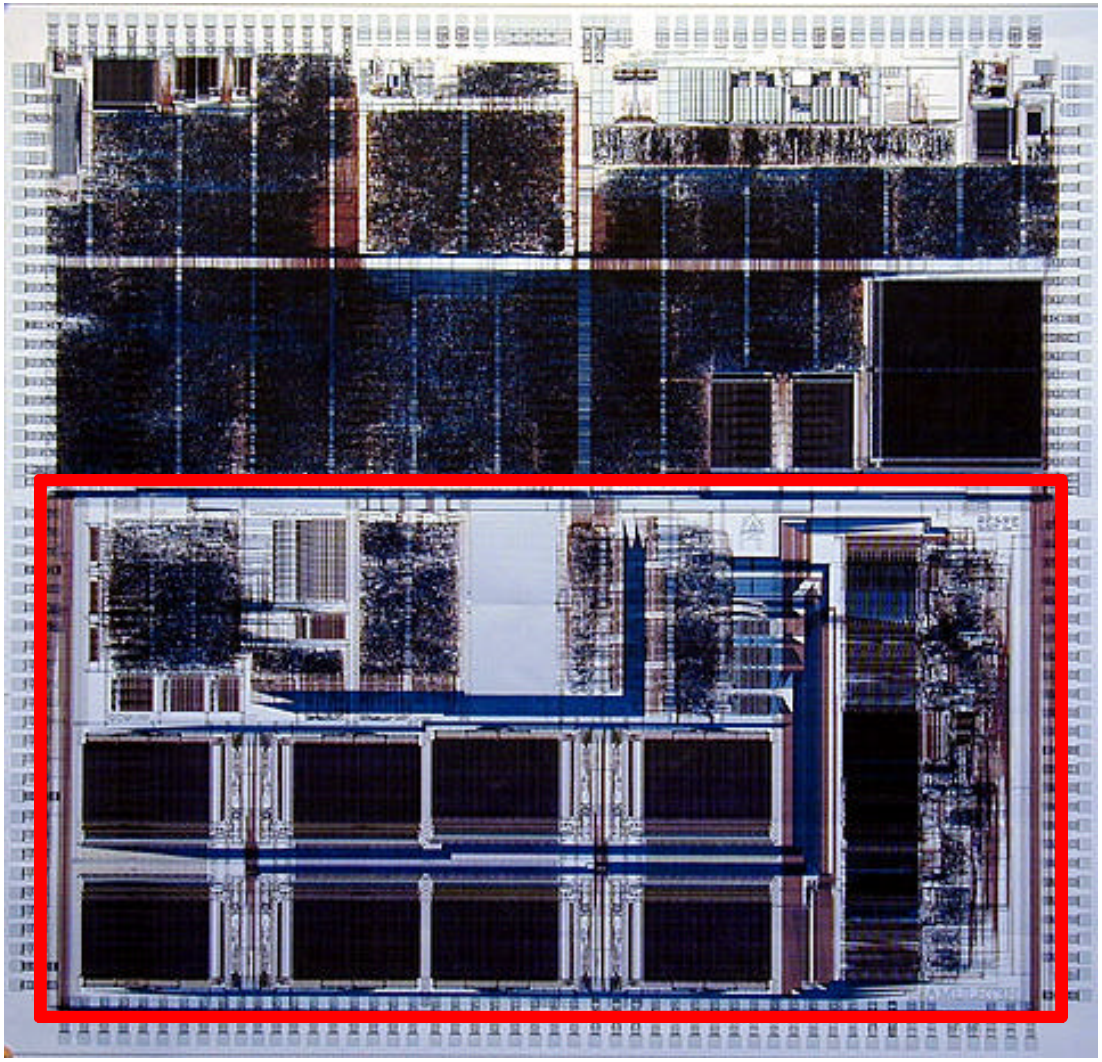
DRACO

- **D**ECT **Ra**dio **Co**mmunications Controller
  - in collaboration with Hagenuk GmbH
  - combines ISDN and DECT telecommunications systems
  - World's first commercial 32-bit asynchronous SoC product
  - volume production this year

DRACO

synchronous peripherals

AMULET3i asynchronous world



Conclusions

- It is feasible to make asynchronous processors which are competitive
- Asynchronous logic offers some real advantages - especially EMC
- Asynchronous logic is becoming commercially interesting